Novel Techniques to Suppress the Common-Mode EMI Noise Caused by Transformer Parasitic Capacitances in DC–DC Converters

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***Abstract*—This paper proposes novel electromagnetic interference (EMI) suppression techniques for dc–dc converters. For low-voltage high-current applications, windings are paralleled and interleaved. Although low conduction loss and low leakage inductance can be achieved, the winding capacitances are considerably increased, thereby deteriorating the converter's EMI and soft-switching performances. To solve these problems, a novel balanced choke concept is proposed, as well as other techniques. The advantages of the proposed concepts and strategies are verified and demonstrated on a 1-kW 1-MHz 400-V/12-V LLC resonant converter prototype. More than 52-dB noise attenuation and 75% equivalent winding capacitance reduction are achieved. Hence, EMI and soft-switching performances are significantly improved.**

***Index Terms*—Common-mode (CM) noise, dc/dc converters, transformer parasitic capacitance.**

I. Introduction

PERFORMANCE-PER-WATT requirements are driving higher efficiency and higher power density metrics in telecommunications, server, and computing equipment design. Hence, there is a large incentive to achieve high efficiency and high power density of power delivery systems [1]–[18]. Front-end converters, which include power factor correction, and dc–dc converters are the key in the whole system. It is required that these applications meet electromagnetic interference (EMI) standards. Normally, EMI filters are required to meet EMI standards. It is essential to achieve low EMI emissions to reduce the size and cost of EMI filters.

For dc–dc converters, multiple parallel windings are widely applied to reduce winding loss. In addition, for isolated applications, interleaving winding structures are preferred to reduce the ac winding loss and leakage inductance. However, large interwinding capacitances become problems because they deteriorate the system performance.

First of all, in terms of EMI, large winding capacitances introduce large common-mode (CM) currents because winding capacitances provide low-impedance paths between the primary and secondary windings; as a result, they deteriorate the system's EMI performance.

Second, in terms of topology, large winding capacitances store energy, and the energy converts to a high voltage spike and high switching loss due to parasitic ringing in hard-switching topologies. For soft-switching topologies, large winding capacitances considerably impair the soft-switching capability. This is discussed later in this paper.

Several noise reduction techniques have been proposed to reduce the CM noise of power converters.

Randomized pulsewidth modulation (PWM) method is used to reduce EMI noise [3]. However, for resonant converters, this method might not be applicable due to different control schemes. Applying a C_z capacitor is another strategy [9]. Shielding is a widely adopted CM noise reduction technique in isolated power converters [4]. It reduces the CM noise by reducing the effective parasitic capacitances associated with the most severe voltage pulsating nodes. However, inserting shielding layers in a transformer introduces additional power loss, and it is not practical in a fully interleaved transformer winding structure since too many shielding layers are needed.

The CM noise of isolated power converters can also be reduced by introducing out-of-phase displacement currents [4], [7]–[11]. In order to achieve full cancellation, either the magnitude of the voltage pulsation or the amount of parasitic capacitances should be controlled. However, in some circumstances, such as in a planar transformer structure, it is not very easy to control either the voltage pulsation or the winding capacitances. Hence, the balanced or compensated capacitances are introduced to cancel the effect of parasitic capacitances. The concept is to generate an out-of-phase CM current to cancel the original CM current on the line impedance stabilization network (LISN). However, for highly interleaved transformer structures, the compensated capacitance is rather large and considerably impairs the soft-switching. This adverse effect of the capacitive compensation is discussed in the following sections.

To solve these problems, this paper studies the EMI and soft-switching performances of dc–dc converters. This study

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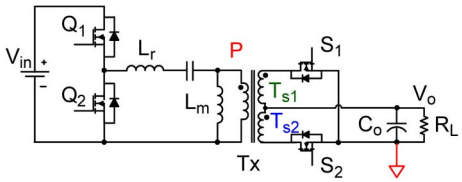

Fig. 1. LLC resonant converter.

particularly reveals the effect of winding capacitances for interleaving windings. Novel balanced choke concepts are proposed to cancel the CM noise of dc–dc converters. Moreover, lumped equivalent winding capacitances can be significantly reduced. Thus, both EMI and circuit performances can be greatly improved.

LLC resonant dc–dc converters exhibit higher efficiency and higher power density characteristics than conventional PWM circuits [1]–[5]. Hence, LLC resonant converters are becoming popular for front-end dc–dc converters in industrial applications, where EN55022 is applied as the common EMI standard. In this paper, the EMI measurements are tested under the guidance of the EN55022. The proposed novel balanced choke techniques and theoretical analysis are verified on a 1-kW 1-MHz 400-V/12-V LLC resonant converter. Furthermore, the proposed methods can be easily extended to other resonant and PWM converters.

II. Winding Capacitances and Their Effect on EMI and Soft-Switching Performances

EMI models of dc–dc converters are studied in [4], [7], and [11]. In an isolated power converter, the interwinding capacitance of the transformer is the critical parasitic capacitance of the converter in terms of CM noise. Such capacitances are distributed along the windings with different voltage pulsations (dv/dt). The interwinding capacitance calculation and the capacitances' effect on EMI are discussed in [7] and [11]. However, the studies are based on spiral windings and a transformer with only two sets of windings. In addition, planar transformers are widely applied. For a planar structure, the primary- and the secondary-side interwinding capacitances are very large due to the large winding area and short face–face distance. For a printed circuit board (PCB) planar structure, interleaving structures further increase the interwinding capacitances. On the other hand, for low-voltage high-current applications, a center-tapped transformer structure is widely adopted. The voltage excitation and distribution are more complicated than those of the transformer with simple two sets of windings.

In this section, the winding capacitances and their effect on EMI and soft switching are discussed. In this paper, a 1-kW 1-MHz 400-V/12-V half-bridge LLC resonant converter is studied as a typical example. This study can be easily extended to other resonant and PWM converters. In this paper, all the EMI measurements are tested under the guidance of the EN55022.

The topology of the half-bridge LLC resonant converter is shown in Fig. 1. The planar transformer structure is adopted due to its low profile, easy manufacture, and its excellent repeatability of properties. The transformer turn ratio used in the

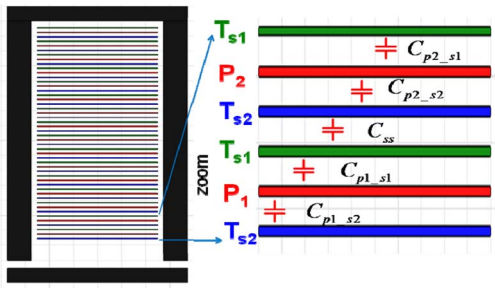

Fig. 2. Half window of an interleaving planar transformer structure and its associated winding capacitances.

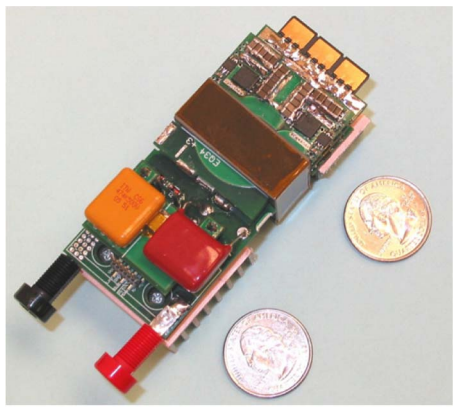

Fig. 3. Prototype of 1-kW 1-MHz 400-V/12-V LLC resonant converter.

prototype is 16:1. Due to very high output current (> 80 A), the secondary side is designed with one turn, and an interleaving structure is selected, which is shown in Fig. 2. The leakage inductance of the transformer is used as L_r in Fig. 1. The primary- and secondary-side windings are designed with one turn per layer. The primary-side windings are connected in series, and the secondary-side windings are connected in parallel. The prototype of the constructed LLC resonant converter is shown in Fig. 3. To save cost, the main board is designed with six-layer PCB. The transformer is constructed with seven six-layer PCB windings plus a six-layer PCB winding on the main board.

A. Parasitic Capacitance Calculation

A simplified parasitic model of the transformer is shown in Fig. 4(a). The leakage inductance L_r and the magnetizing inductance L_m are utilized as the resonant tank magnetic elements. The lumped L_r and L_m are shown in Fig. 4(a). $C_{\rm ps}$ is modeled as the interwinding capacitances. $C_{\rm pp}$ is modeled as the primary-side intrawinding capacitances, and $C_{\rm ss}$ is modeled as the secondary-side intrawinding capacitances. The distributed stray interwinding capacitances are shown in Fig. 4(b). C_{pm_s1} and C_{pm_s2} represent unit interwinding capacitances (from the mth layer of primary-side winding to one secondary-side winding). For the sake of convenience, the lumped winding capacitances are derived in (1)–(15).

Because only dv/dt generates capacitive current, the ground point position does not alter the value of the winding capacitances. Hence, the ground point can be equivalently shifted

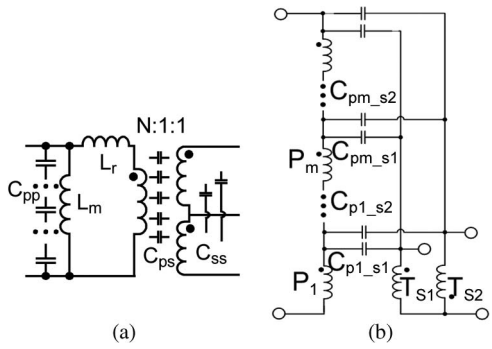

Fig. 4. Simplified parasitic models for transformer: (a) The parasitic model of the transformer and (b) interwinding capacitances of the transformer.

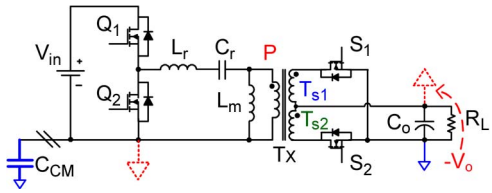

Fig. 5. Equivalent ac ground of the LLC resonant converter.

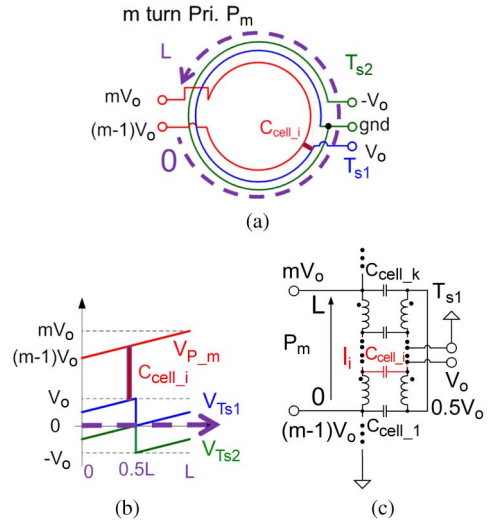

Fig. 6. Physical layout, voltage distribution, and equivalent distributed interwinding capacitance model of one interleaving cell of transformer windings: (a) The simplified physical layout of one interleaving cell of the transformer winding, (b) the voltage distribution of one interleaving cell of the transformer winding, and (c) the equivalent distributed interwinding capacitance model of one cell winding (C_{pm_s1}).

and is shown in Fig. 5. The original V_o is the new equivalent ground point, and the original ground turns to $-V_o$. In this way, it is more convenient to calculate the parasitic capacitance due to the symmetrical ac voltage excitation on the secondary windings. Also, it is assumed that the CM capacitor (Y-cap) is larger than the parasitic capacitances. Thus, the primary side is considered virtually grounded. The PCB transformer windings are wound circularly. The voltage distribution of the primary- and the secondary-side windings is shown in Fig. 6. Because there is one turn per layer for both the primary- and secondary-side windings, the voltage gradients on each layer are the same.

There are several strategies for calculating the lumped stray capacitances. One is the equivalent energy method, and another

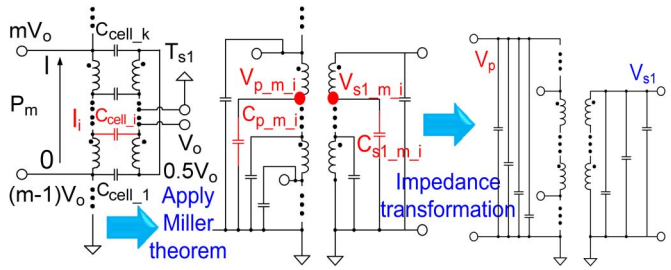

Fig. 7. Illustration of the derivation of one unit of interwinding capacitances C_{pm_s1} (from the mth layer of the primary-side winding to one secondary-side winding) based on Miller theorem.

is equivalent charge or Cdv/dt [1]–[7], [13], [14]. The second method is to be used in this paper because of its convenience. In this paper, the equivalent electrical circuit of the parasitic capacitance is derived based on the Miller theorem. Shown in Fig. 7, C_{pm_s1} and C_{pm_s2} are derived. The basic idea is to perform the following: 1) to equivalently transfer the interwinding capacitance into intrawinding capacitance according to the Miller theorem; 2) to calculate the unit terminal capacitance of the mth-layer interwinding capacitance according to the impedance transformation of the transformer; and 3) to obtain the lumped capacitance from the summed unit terminal capacitance of every layer of interwinding capacitances.

The parasitic capacitances and the PCB winding structure are shown in Fig. 2. It is assumed that the voltage of the transformer winding is evenly distributed. Due to a very weak capacitive coupling, $C_{\rm pp}$ is very small and can be ignored. As shown in Fig. 7, the interwinding capacitance is derived as follows: $C_{\rm cell}$ is an illustrative cell of physical interwinding capacitance without consideration of voltage excitation. According to (1), the voltage gain of the ith cell of the mth layer of the primary-side winding to the secondary-side winding T_{s1} can be calculated. Based on the Miller theorem, from (2) and (3), the interwinding capacitance can be decoupled as the intrawinding capacitances. Then, according to transformer impedance transformations (4) and (5), $C_{p\_m\_i}$ and $C_{s1\_m\_i}$ can be equivalently expressed as the primary- and the secondary-side terminal winding capacitances. For the sake of convenience, the secondary-side winding capacitances can be further transformed to the primary-side winding capacitances

$$A_{m\_i} = \frac{V_{s1\_m\_i}}{V_{p\_m\_i}} \tag{1}$$

$$C_{p\_m\_i} = C_{\rm cell}(1 - A_{m\_i}) \tag{2}$$

$$C_{s1\_m\_i} = C_{\rm cell}(1 - 1/A_{m\_i}) \tag{3}$$

$$C_{p\_m\_i\_\rm lumped} = C_{p\_m\_i}\left(\frac{V_{p\_m\_i}}{V_p}\right)^2 \tag{4}$$

$$C_{s1\_m\_i\_\rm lumped} = C_{s1\_m\_i}\left(\frac{V_{s1\_m\_i}}{V_{s1}}\right)^2. \tag{5}$$

Finally, the distributed capacitances can be summed together, and the lumped terminal capacitances can be obtained.

The physical layer-to-layer capacitance $C_{\rm unit}$ is expressed in (6), where $\varepsilon_{\rm PCB}$ is the permittivity of the PCB material, $A_{\rm PCB}$ is the PCB copper area of one turn winding, d_{ly} is

the winding-to-winding distance, and l_i is the location of the ith-cell capacitance. N is the primary-side turn number. The voltage gain between the primary- and secondary-side windings A_{m_li} is calculated in (7). According to the Miller theorem, (8) and (9) equivalently transfer the interwinding capacitance into the primary-side capacitance $\Delta C_{p\_m\_li}$ and the secondary-side intrawinding capacitance $\Delta C_{s1\_m\_li}$, respectively. Based on the impedance transformation of the transformer, they can be lumped into the primary-side terminal winding capacitances. Transformed to the primary-side terminals, $C_{p\_m\_\mathrm{lumped}}$ and $C_{s1\_m\_\mathrm{lumped}}$ are the sums of $\Delta C_{p\_m\_li}$ and $\Delta C_{s1\_m\_li}$ on the mth layer, respectively. $C_{\mathrm{ps1}\_m\_\mathrm{lumped}}$ is the total interwinding capacitances of the mth layer transformed to the primary-side terminals. In (13), the overall interwinding capacitances $C_{\mathrm{ps\_tot\_lumped}}$ transformed to the primary-side terminals are expressed. The secondary-side intrawinding capacitance $C_{\mathrm{ss\_lumped}}$ transformed to the primary side is obtained in (14)

$$C_{\mathrm{unit}}=\frac{\varepsilon_0\varepsilon_{\mathrm{PCB}}\cdot A_{\mathrm{PCB}}}{d_{ly}} \tag{6}$$

$$A_{m\_li}=\frac{V_{p\_m\_i}}{V_{s1\_m\_i}}=\begin{cases}\frac{0.5V_o+V_ol_i/l}{(m-1)V_o+V_ol_i/l}, & \text{if } l_i\le 0.5l\\ \frac{-0.5V_o+V_ol_i/l}{(m-1)V_o+V_ol_i/l}, & \text{if } l_i>0.5l\end{cases} \tag{7}$$

$$\Delta C_{p\_m\_li}=(1-A_{m\_Li})\frac{\Delta l_i}{l}C_{\mathrm{unit}} \tag{8}$$

$$\Delta C_{s1\_m\_li}=\begin{cases}\left(1-\frac{1}{A_{m\_li}}\right)\frac{\Delta l_i}{l}C_{\mathrm{unit}}, & \text{if } l_i\le 0.5l\\ \left(1-\frac{1}{A_{m\_li}}\right)\frac{\Delta l_i}{l}C_{\mathrm{unit}}, & \text{if } l_i>0.5l\end{cases} \tag{9}$$

$$C_{p\_m\_\mathrm{lumped}}=\frac{C_{\mathrm{unit}}}{l}\int_0^l(1-A_{m\_li})\left(\frac{m-1+l_i/l}{N}\right)^2 dl_i \tag{10}$$

$$C_{s1\_m\_\mathrm{lumped}}=\frac{C_{\mathrm{unit}}}{l}\Bigg[\int_0^{0.5L}\left(1-\frac{1}{A_{m\_li}}\right)\left(\frac{0.5+l_i/l}{N}\right)^2 dl_i+\int_{0.5l}^{l}\left(1-\frac{1}{A_{m\_li}}\right)\left(\frac{-0.5+l_i/l}{N}\right)^2 dl_i \tag{11}$$

$$C_{\mathrm{ps1}\_m\_\mathrm{lumped}}=C_{p\_m\_\mathrm{lumped}}+C_{s1\_m\_\mathrm{lumped}} \tag{12}$$

$$C_{\mathrm{ps\_tot\_lumped}}=\sum_{m=1}^{N}(C_{\mathrm{ps1}\_m\_\mathrm{lumped}}+C_{\mathrm{ps2}\_m\_\mathrm{lumped}})=\sum_{m=1}^{N}\frac{4m^2-4m+3}{2N^2}C_{\mathrm{unit}} \tag{13}$$

$$C_{\mathrm{ss\_lumped}}=\sum_{m=1}^{N-1}C_{\mathrm{ss}\_m\_\mathrm{lumped}}=\sum_{i=1}^{N-1}\frac{C_{\mathrm{unit}}}{N^2} \tag{14}$$

$$C_{\mathrm{trans\_lumped}}=C_{\mathrm{ss\_lumped}}+C_{\mathrm{ps\_tot\_lumped}}. \tag{15}$$

B. Impacts of Parasitic Capacitance on EMI Characteristics

Based on (13), the lumped interwinding capacitance $C_{\mathrm{ps\_tot\_lumped}}$ is 935 pF. In [4], a detailed CM noise model of LLC resonant converters is studied. The parasitic parameters of active and passive components, transformers, heat sinks, and noise source characteristics have been analyzed in detail.

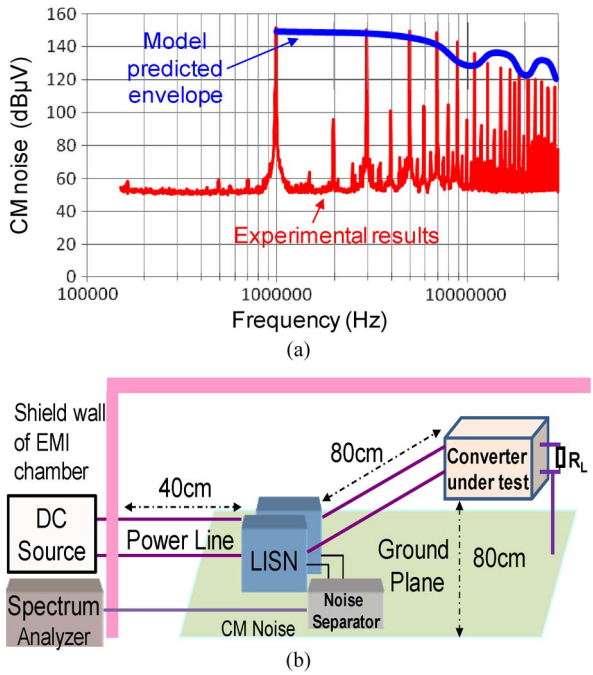

Fig. 8. Measured EMI spectrum and the measurement setup of the constructed 1-kW 1-MHz 400-V/12-V LLC prototype: (a) Measured and predicted EMI spectrum of the prototype and (b) EMI measurement setup.

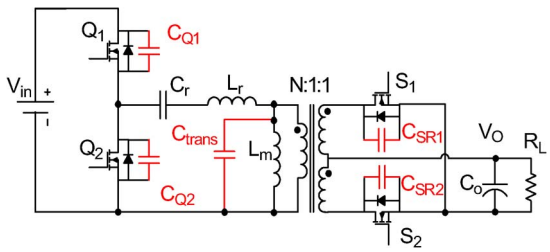

Fig. 9. Impacts of parasitic capacitances on soft-switching characteristics.

According to the EMI model proposed in [4], the CM noise spectra are evaluated and compared with the experimental results, which are shown in Fig. 8(a). The EMI measurement setup is shown in Fig. 8(b). The predicted EMI performance is very close to the measured performance. The CM noise is very high due to the large interwinding capacitance. The predicted EMI performance is more accurate in the relatively low frequency area (<8 MHz). In the high-frequency area, the lumped model might not be accurate enough to predict the whole EMI spectrum. However, normally, for EMI designers, the accuracy of the low-frequency area might be more critical for EMI filter design. The detailed explanation of the discrepancy is addressed in [4].

C. Impacts of Parasitic Capacitance on Soft-Switching Characteristics

On the other hand, the large winding capacitances considerably affect the soft-switching performance. Based on (15), $C_{\mathrm{trans\_lumped}}$ is 941.4 pF. The parasitic capacitances include the primary-side device junction capacitance, the synchronous rectifier (SR) junction capacitance, and the winding stray capacitances. Figs. 9 and 10 show the parasitic capacitances and

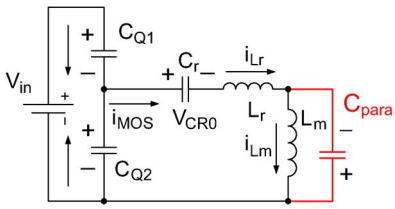

Fig. 10. Equivalent circuit during the soft-switching transition.

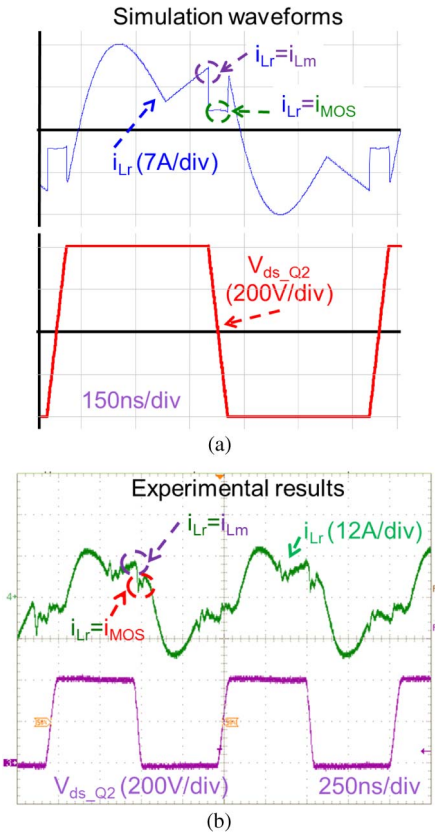

Fig. 11. Impacts of winding capacitances on ZVS performance: (a) Simulated waveforms and (b) experimental waveforms.

the equivalent circuit during the soft-switching transition time. The total primary-side junction capacitances are 370 pF. The total SR junction capacitances transformed to the primary side are 140 pF. $C_{\rm para}$ is the sum of the transformer stray capacitances and the transformed total SR junction capacitances

$$C_{\rm para} = C_{\rm trans\_lumped} + C_{\rm SR\_lumped}. \tag{16}$$

According to Fig. 10, during the soft-switching transition time, $C_{\rm para}$ shunts the magnetizing current, which is critical to achieve zero-voltage switching (ZVS). Due to very large transformer stray capacitances, only a small amount of the magnetizing current is utilized to achieve ZVS. In Fig. 11, the simulated waveforms and the experimental results clearly illustrate that almost two-thirds of the magnetizing current is diverted by the transformer parasitic capacitances. To achieve full ZVS, the magnetizing current has to increase three times. The conduction loss increases significantly. This is a detrimental side effect of large transformer parasitic capacitances.

It should be noted that the conventional interwinding capacitance measurement, which is shown in Fig. 12, is used to

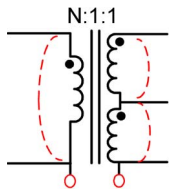

Fig. 12. Conventional measurement for interwinding capacitance.

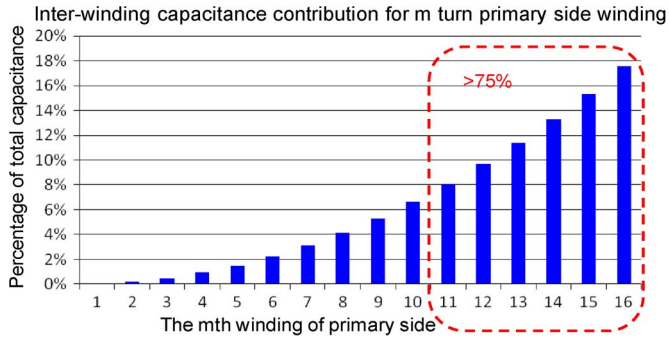

Fig. 13. Interwinding capacitance contribution for different turns of primary-side windings.

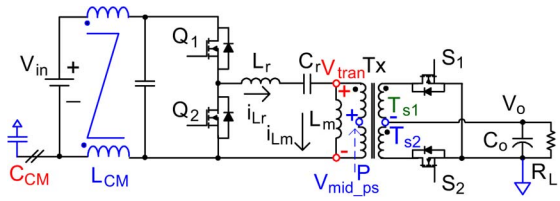

Fig. 14. Proposed CM choke to reduce equivalent interwinding capacitances.

measure the capacitances between the short primary- and the secondary-side windings. The measured capacitance is 2.98 nF. The calculated physical capacitance is 2.79 nF. This suggests that the direct measured winding capacitance should not be adopted. The indirect measurement is to compare the currents during ZVS transition time. Hence, a winding capacitance of 969 pF is derived based on the measured current waveforms, which validates the modeled winding capacitances.

III. Proposed CM Choke Method to Reduce Equivalent Parasitic Capacitances

Based on (13), the lumped interwinding capacitance of each cell of the primary-side winding can be calculated. The results are shown in Fig. 13. Due to the high dv/dt effect, the primary-side windings with higher voltage contribute more to the equivalent capacitances. The 11th–16th windings contribute more than 75% of the total interwinding capacitances. To reduce the equivalent winding capacitances, these primary-side windings can be designed with a noninterleaving structure. However, this leads to a higher winding loss.

The current flowing through $C_{\rm para}$ in Fig. 10 includes the CM noise current which flows from the primary to the secondary, to the CM capacitors in the secondary, to the ground, to the input CM capacitors, and back to the primary. As shown in Fig. 14, we propose adding a CM choke $L_{\rm CM}$ to reduce both equivalent winding capacitances and CM noise. The input

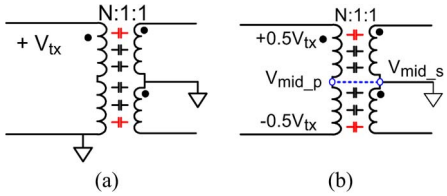

Fig. 15. Virtual ac ground point comparison with and without the proposed CM choke: (a) Virtual ac ground without the proposed CM choke and (b) virtual ac ground with the proposed CM choke.

current is very low for a 1-kW converter at 2.5 A. Thus, the CM choke can be designed to be very small with a very low loss.

The detailed calculation of equivalent interwinding capacitances is provided in Section II-A. The physical interwinding capacitance is calculated in (6). Without changing the physical dimension or structure of the transformer, the physical capacitance does not change. However, as studied in Section II-A, the CM current is strongly related to the voltage distribution [13], [14]. Fig. 6 shows the voltage distribution of the individual winding. Equations (7)–(15) show how to obtain the equivalent capacitances in terms of CM current calculation. Furthermore, the equivalent interwinding capacitance of each cell of the primary-side winding is calculated. Fig. 13 shows how voltage distribution impacts the equivalent parasitic interwinding capacitance. Due to the high dv/dt effect (or more energy stored between the windings), the primary-side windings with higher voltage contribute more to the equivalent capacitances. The equivalence lumped capacitance reflects the impact on the CM current.

For the original dc–dc converter, which has a large CM capacitor, the virtual ac ground point is shown in Fig. 15(a). With $L_{\rm CM}$, the virtual ac ground point is moved to the middle point of the primary-side winding, which is shown in Fig. 15(b). $V_{\rm mid\_ps}$ is the voltage across the middle points of the primary- and secondary-side windings. $V_{\rm mid\_ps}$ is captured experimentally and verified in Fig. 16. As a result, the voltage across the primary- and the secondary-side windings is redistributed. The equivalent interwinding capacitance is recalculated in (17). The capacitive stored energy is proportional to the square of the voltage. Due to the lower voltage excitation across the primary- and the secondary-side windings, the equivalent interwinding capacitance is reduced to 237 pF, which means a 75% reduction. The experimental results verify the equivalent capacitance reduction. With the lower equivalent winding capacitance, the required magnetizing current for ZVS is reduced. Hence, lower circulating current and lower conduction loss are achieved

$$C_{\rm ps\_tot\_lumped} = \sum_{m=1}^{\frac{N}{2}} \frac{4m^2 - 4m + 3}{N^2} C_{\rm unit}. \qquad (17)$$

When $L_{\rm CM} = 200\ \mu$H, the CM noise can be greatly reduced as well. A simplified EMI model of the original dc–dc converter is shown in Fig. 17(a), and a simplified EMI model of the improved LLC dc–dc converter is shown in Fig. 17(b). The CM currents of the original and the improved LLC dc–dc converter are shown in Fig. 18. The CM current of the improved circuit can be calculated in (18). If the impedance of $L_{\rm CM}$ is much larger than the impedance of the equivalent interwinding capacitance, the CM noise current can be calculated in (19). The predicted CM noises match the experimental results very well, as shown in Fig. 19

$$i_{\rm CM} = \frac{V_{\rm tran}}{Z_{Cps1} + \frac{Z_{Cps2} Z_{Lcm}}{Z_{Cps2} + Z_{Lcm}}} \frac{Z_{Cps2}}{Z_{Cps2} + Z_{Lcm}} = \frac{V_{\rm tran}}{Z_{Cps2} + 2Z_{Lcm}} \qquad (18)$$

$$i_{\rm CM}(t) = \frac{NV_oT_s}{16L_{\rm CM}} \frac{2}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n^2} \cos\left(\frac{2n\pi}{T_s} t\right). \qquad (19)$$

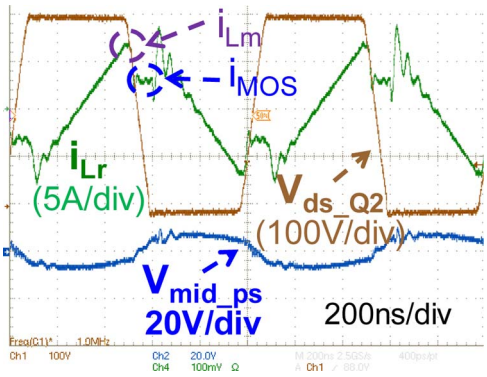

Fig. 16. Experimental results of the improved ZVS operation with the proposed CM choke at no-load condition.

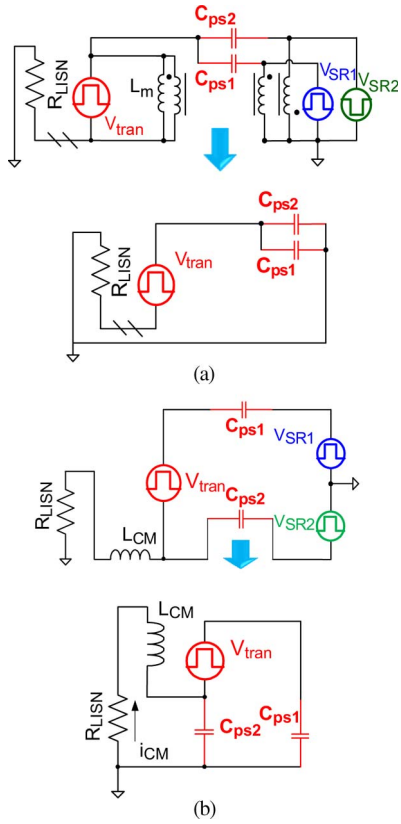

Fig. 17. Simplified EMI model comparison with and without the proposed CM choke: (a) The simplified EMI model of the original LLC converter and (b) the simplified EMI model with the proposed CM choke.

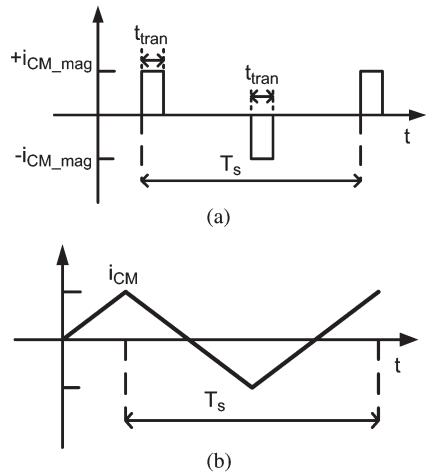

Fig. 18. CM current comparison for LLC resonant converter with and without the proposed CM choke: (a) The CM current of the original LLC resonant converter and (b) the CM current of the LLC resonant converter with the proposed CM choke.

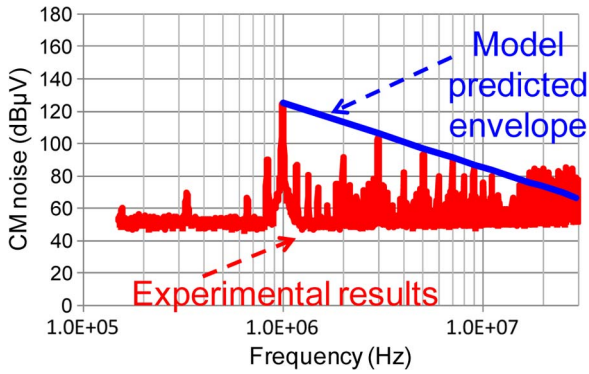

Fig. 19. Measured EMI spectrum and the predicted EMI spectrum envelope of the LLC prototype with the proposed CM choke.

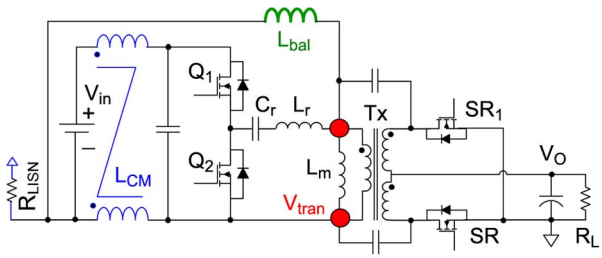

Fig. 20. Novel proposed balanced choke topology to cancel EMI noise of dc–dc converters.

IV. Proposed Balanced Choke Concept to Reduce Equivalent Parasitic Capacitances and CM Noise

With the proposed CM choke, both the EMI and soft-switching performances are improved. However, the CM noise is still high. According to (19), the CM current is related to the inductance of $L_{\rm CM}$. To further improve the EMI performance, we propose novel balanced choke techniques. Shown in Fig. 20, another balanced choke $L_{\rm bal}$ is inserted. The simplified EMI model is shown in Fig. 21. Once (20) is satisfied, a balanced Wheatstone bridge network [10] is generated. Hence, the voltage drop on the LISN resistor should be zero. Ideally, the CM

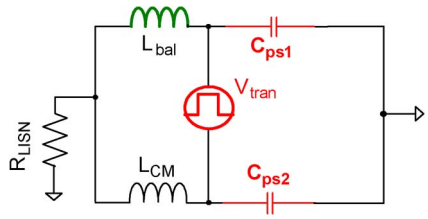

Fig. 21. Equivalent EMI model of the balanced network to cancel CM noises with the proposed balanced choke techniques.

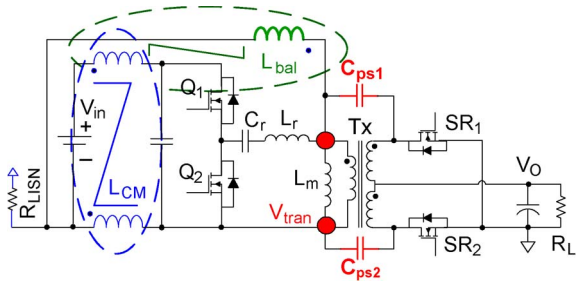

Fig. 22. Proposed novel coupled balanced choke topology to cancel EMI noises of dc–dc converters.

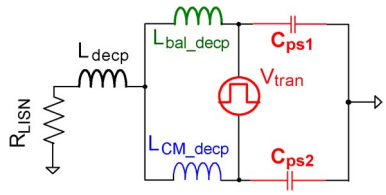

Fig. 23. Equivalent EMI model of the coupled balanced network to cancel CM noises with the proposed coupled balanced choke techniques.

noise should be canceled. Compared with the proposed CM choke technique, the balanced choke concept does not require high inductance to achieve low EMI noise. Also, more CM noise attenuation can be obtained

$$L_{\rm bal}/L_{\rm CM} = C_{\rm ps2}/C_{\rm ps1} \Rightarrow i_{\rm CM} = 0. \tag{20}$$

To further simplify the circuit, it is proposed to integrate $L_{\rm bal}$ with $L_{\rm CM}$. Shown in Fig. 22, $L_{\rm bal}$ can be coupled with $L_{\rm CM}$. Since $L_{\rm bal}$ does not carry any dc current, it is very easy to couple all the magnetic components into one small core.

The EMI model of the balanced coupled choke is shown in Fig. 23, where $L_{\rm bal\_decp} = L_{\rm bal} + k\sqrt{L_{\rm bal} \cdot L_{\rm CM}}$, $L_{\rm CM\_decp} = L_{\rm CM} + k\sqrt{L_{\rm bal} \cdot L_{\rm CM}}$, and $L_{\rm decp} = -k\sqrt{L_{\rm bal} \cdot L_{\rm CM}}$, with k being the coupling coefficient.

Fig. 24 shows the measured CM noise spectrum. With $L_{\rm CM} = 104\ \mu$H and a 15:15:15 turn ratio of the balanced coupled choke, the CM noise is attenuated. Due to the mismatch of the equivalent interwinding capacitances, the EMI attenuation is limited.

To compensate the mismatch of equivalent interwinding capacitances, an unsymmetrical coupled balanced choke can be designed. The coupling turn ratio is readjusted as 15:14:14. Hence, it is closer to achieving the conditions in (20). In this case, 17-dB attenuation is obtained compared with the CM choke technique. Fig. 24 shows the results.

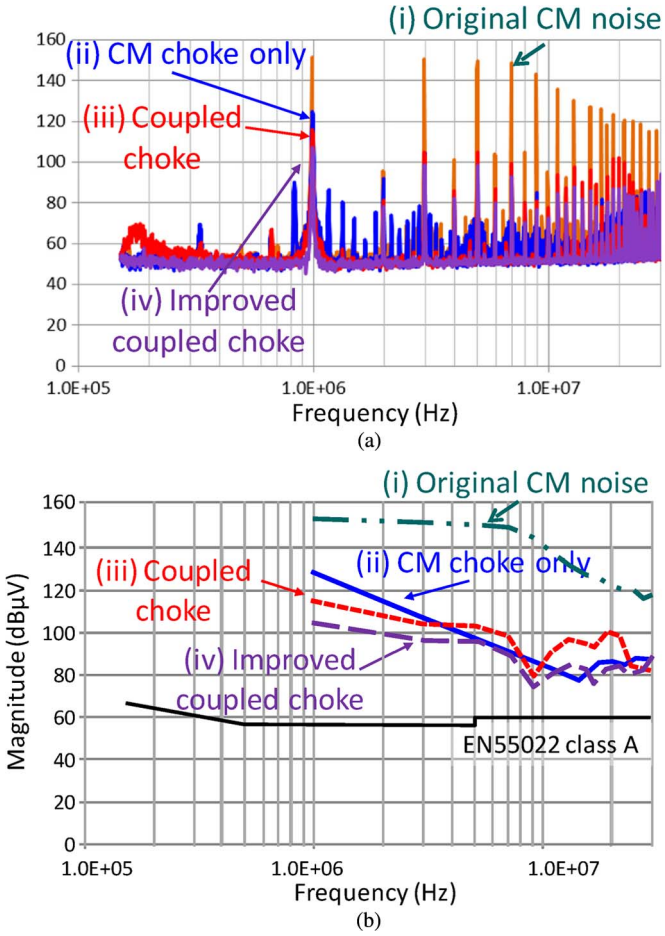

Fig. 24. Measured EMI spectrum comparison for the proposed choke techniques: (a) Measured EMI and (b) envelope of the measured EMI. (i) Original CM noise, (ii) with the CM choke only, (iii) with the coupled balanced choke of unit couple turn ratio, and (iv) with the coupled balanced choke of the nonunit coupled turn ratio.

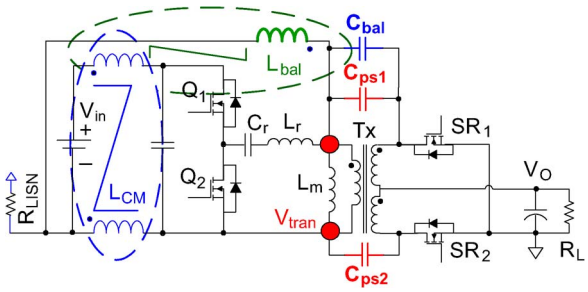

Fig. 25. Improved novel balanced choke and balanced capacitor topology to cancel the EMI noise of dc–dc converters.

To more closely match (20) and further reduce CM noise, we propose a combined balanced coupled choke and balanced capacitor concept, which is shown in Fig. 25. The equivalent EMI model is shown in Fig. 26. With the proposed balanced capacitor $C_{\rm bal}$, a balanced network can be obtained easily. There are two methods of balanced network refinement. The simplest way is to keep the same turn ratio and directly balance the equivalent interwinding capacitances, namely, $C_{\rm ps1} + C_{\rm bal} = C_{\rm ps2}$. Another way is to adjust the turn ratio of the balanced choke unevenly and add the necessary $C_{\rm bal}$ to balance the converter network.

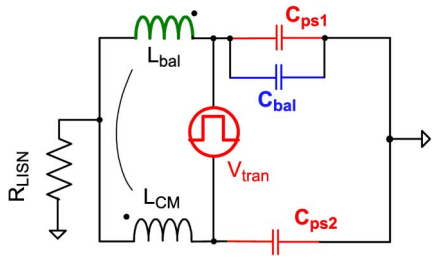

Fig. 26. Equivalent EMI model of the improved coupled balanced network to cancel CM noise with the proposed coupled balanced choke and balanced capacitor techniques.

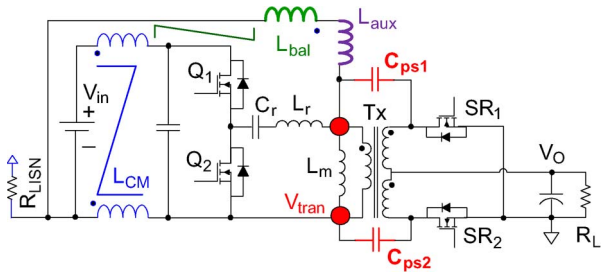

Fig. 27. Improved balanced choke network to cancel EMI noise.

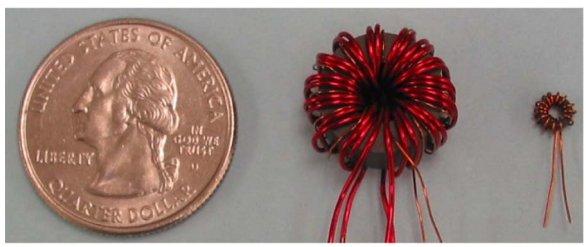

Fig. 28. Pictures of the proposed coupled balanced choke and the auxiliary balanced choke for the 1-kW 1-MHz 400-V/12-V LLC resonant converter: U.S. quarter dollar on the left, the coupled balanced choke in the middle, and the auxiliary balanced choke on the right.

Simplicity and easy implementation are key advantages when combining balanced coupled choke and balanced capacitor concepts. Nevertheless, in some circumstances, where the inserted balanced capacitance is too large, it may introduce a slightly adverse effect on ZVS performance. To avoid any extra capacitive current, we propose an improved balanced choke network, which is shown in Fig. 27. With an extra auxiliary tiny inductor $L_{\rm aux}$, more freedom is achieved to refine the CM balanced network and cancel the CM noise.

The balanced coupled choke and the auxiliary balanced choke are designed with toroid cores. Prototypes of the balanced chokes are shown in Fig. 28. As mentioned before, the balanced CM choke carries very low input dc current. The balanced chokes $L_{\rm bal}$ and $L_{\rm aux}$ do not conduct any dc current and only conduct very small ac current. Therefore, the total loss of the balanced chokes is very small, and a very compact design is easily accomplished. The estimated total loss of the balanced choke is around 1.4 W at 1-kW full-load conditions. Furthermore, the proposed balanced choke is essential to reducing the equivalent interwinding capacitances. It is very helpful for the soft switching and the reduction of circulating current.

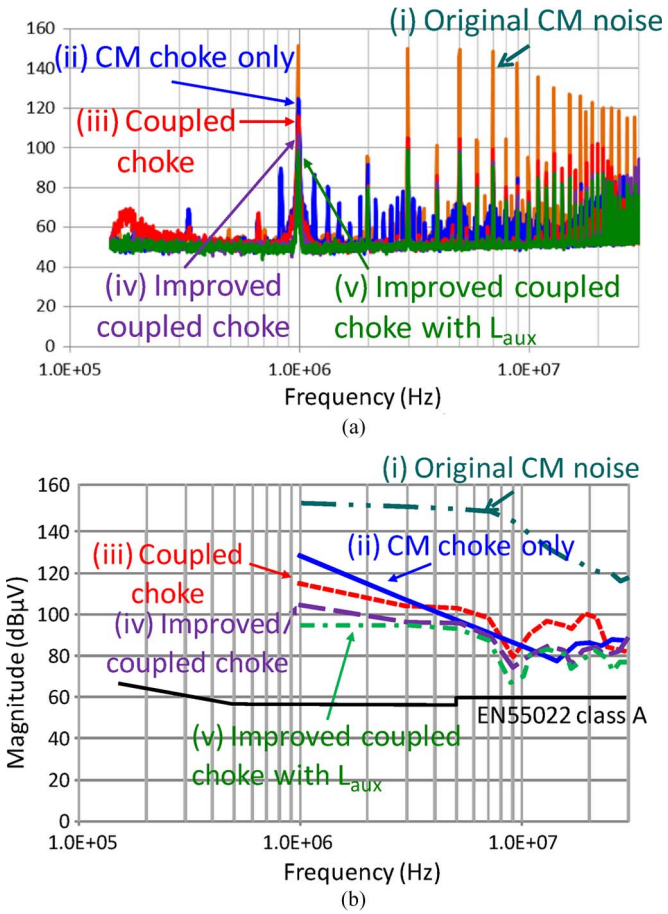

Fig. 29. Comparison of measured EMI spectrums for the proposed choke techniques: (a) Measured EMI and (b) envelope of the measured EMI. (i) Original CM noise, (ii) with the CM choke only, (iii) with the coupled balanced choke of unit couple turn ratio, (iv) with the coupled balanced choke of nonunit couple turn ratio, and (v) with the combined auxiliary balanced choke and the coupled balanced choke.

The measured EMI spectrum is provided and compared with other proposed EMI reduction schemes in Fig. 29. Compared with the proposed CM choke scheme, 27-dB attenuation is obtained. Compared with the original LLC dc–dc converters, more than 52-dB attenuation is achieved.

The objective of this paper is to propose a different approach to reduce CM EMI. The EMI filter design is not the scope. Therefore, EMI filter sizes before and after applying the proposed solutions are not compared. In principle, using the balanced network to reduce EMI is totally different from using EMI filters [8]. For an EMI filter, the EMI attenuation is based on the corner frequency of the filter. Nevertheless, the balanced network strategy utilizes the balanced impedance network to cancel EMI noise. Hence, a smaller balance component can achieve the same attenuation as a much larger EMI filter [8]. For a conventional EMI filter, its corner frequency is determined by the low-frequency EMI noise [15], [16]. The proposed solution greatly reduces low-frequency noise, so the corner frequency of the CM EMI filter can be greatly increased. As a result, much smaller filter size can be achieved. In addition, in this paper, the added CM inductor $L_{\rm CM}$ carries much smaller dc current at 400-V dc side than conventional filters with ac current at 120-V ac input side. The thickness of winding wires is reduced considerably. This leads to more size reduction and loss reduction than the conventional filter design on the ac side.

The conventional CM choke can reduce the CM noise but with significantly large CM inductance. According to Fig. 29, the proposed coupled CM choke and balanced network strategy can provide pronounced noise suppression without large inductance value. In particular, the proposed methods can greatly strengthen the noise attenuation with very small CM choke.

For practical applications, the tolerance of the inductance and the parasitic capacitance may impact the noise attenuation performance. An optimal coupling turn ratio (nonunity turn ratio) should be chosen to offset the given manufactory or layout nonideality or asymmetry. According to Fig. 29, it is clear that, the less the mismatch, the more significant the noise attenuation. With the extra auxiliary inductor, more noise reduction can be achieved. Nevertheless, without the auxiliary inductor, the attenuation is still pronounced. The better tradeoff should be made among tolerance, EMI filter size, and cost. This paper provides alternate strategies to improve the practical design.

The proposed concepts and strategies can be easily extended to other PWM and resonant topologies. The benefits of reducing equivalent winding capacitances and attenuating CM noise can be achieved for both soft- and hard-switching converters. For soft-switching applications, less circulating current is needed to achieve ZVS. For hard-switching applications, less capacitive energy is dissipated. The proposed techniques are essentially beneficial for the applications, in which interleaving transformers are used. The adverse effect of large interwinding capacitances can be significantly attenuated.

V. Conclusion

This paper has provided a thorough study of the impacts of winding capacitances on soft-switching performance and EMI noise. Several novel concepts and techniques have been proposed to reduce the lumped equivalent parasitic interwinding capacitances and EMI noise. With the proposed balanced coupled choke concept, the lumped equivalent parasitic interwinding capacitance can be reduced by 75%, and more than 52-dB CM noise attenuation is achieved. The current required for soft switching is reduced considerably, and conduction loss is reduced accordingly.

Finally, the theoretical analysis and the proposed techniques are verified on a 1-MHz 1-kW LLC resonant converter prototype. The prototype exhibits low EMI noise and easily accomplished soft-switching characteristics. The theoretical analysis methodology and the proposed novel techniques can be easily extended to other resonant and PWM converters.

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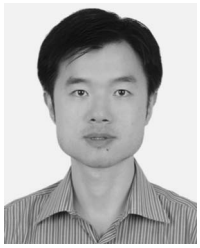

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